REMARKS

Claims 41-67 are pending in the present application.

In the office action mailed March 11, 2004 (the "Office Action") claims 41-43, 45-48, and 54-64 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,134,681 to Akamatsu et al. (the "Akamatsu patent") in view of Hancu et al., "A Concurrent Test Architecture For Massively Parallel Computers and Its Error Detection Capability," IEEE Transactions on Parallel and Distributed Systems, pp. 1169-84, Vol. 5, Issue 11 (the "Hancu article") and Park et al., "Address Compression Through Base Register Caching," IEEE, pp. 193-199, 27-29 November 1990 (the "Park article"). Claims 44, 49-53, and 65-67 were rejected under 35 U.S.C. 103(a) as being unpatentable over various combinations of the Akamatsu patent in view of the Hancu article and the Park article. More specifically, in further view of U.S. Patent No. 4,642,793 to Meaden (the "Meaden patent"), or in further view of U.S. Patent No. 5,659,737 to Matsuda (the "Matsuda patent"), or in further view of IBM technical disclosure bulletin entitled, Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory, June 1, 1988 (the "IBM technical disclosure").

Claims 41, 45, 47, 49, 54, 55, 64, and 65, have been amended herein to clarify the subject matter of the claims, since it appears that there has been some difficulty for the Examiner in understanding the invention. It will be apparent from the amendments, and the comments below, that the amendments were made independent of the cited references. None of previously mentioned amendments narrow or further limit the scope of the invention as recited by the respective claim. Generally, the amendments make explicit what is implicit in the claim, add language that is inherent in the unamended claim, or merely redefine a claim term that is previously apparent from the description in the specification. Consequently, the amendments should not be construed as being "narrowing amendments," because these amendments were not made for a substantial reason related to patentability.

In rejecting the pending claims, the Examiner has merely raised the same rejections to the claims as found in the previous office actions, except that yet another reference is being relied upon, namely, the Park article. As will be discussed in more detail below, however, one ordinarily skilled in the art would not be motivated to combine the teachings of the Park article, or any of the secondary references cited by the Examiner, with the Akamatsu patent.

Additionally, even if the teachings of the Park article were combined with the cited references, the Park article does not make up for the deficiencies of the Akamatsu patent, the Hancu article, the Meaden patent, the Matsuda patent, and the IBM technical disclosure, as discussed in great detail in the previously filed responses. The combination of any of these references with the Akamatsu patent fails to teach or suggest the combination of limitations recited by the respective claims.

The Examiner has found another a reference that is directed to address compression at a system level, and is attempting to apply its teachings to the Akamatsu patent in order to substantiate an obviousness rejection of the present claims. As explained in the previously filed responses, the Akamatsu patent is specifically directed to reducing access times of a memory device by selecting a column of memory for access sooner if none of the redundant columns of memory are used for an array than if redundant columns of memory have been used in the memory array. Of significance is the fact that the Akamatsu patent is specifically directed to the internal timing and operation of a memory device. In contrast, the Park article is directed to a method of compressing addresses in order to reduce processor-to-memory bandwidth. As expressly stated in the Park article, the method disclosed in the article is focused "specifically on reducing bandwidth requirements between processor and memory" See p. 193, col. 1, second paragraph under "Introduction" (emphasis added). The base register caching method of address compression described in the Park article requires base register hardware at the processor and at the memory. See p. 196, under "Implementation Issues." The Akamatsu patent does not describe a processor at all. Nor does the Akamatsu patent mention address compression at all. As known by those ordinarily skilled in the art, "address compression" is not used internally in a memory device as part of the redundancy memory scheme. Consequently, one ordinarily skilled in the art would not be motivated to combine the teachings of the Akamatsu patent, which are directed to early column access for a memory device having a redundant memory scheme, with the references teaching various methods of address and data compression, cited by the Examiner. This is clearly the case with the Park article since it is directed to a method of address compression wholly inapplicable to redundant memory remapping in a memory device.

Moreover, the combined teachings of the Akamatsu patent with the Hancu article, the Park article, the Meaden patent, the Matsuda patent, or the IBM technical disclosure fail to disclose the combination of limitations recited by the respective claims. As explained in the

Appl. No. 09/695,756

previously filed responses, the Akamatsu patent fails to disclose methods as recited in the respective claims as characterized by the Examiner. The Park article, as previously discussed, merely describes a method for base register caching for reducing processor-to-memory bandwidth. As with the other secondary references previously cited by the Examiner, the Park article fails to make up for the fundamental deficiencies of the Akamatsu patent explained in the earlier filed responses. Rather than repeat the same arguments in the present response, the Examiner is directed to the remarks of the earlier filed responses detailing the deficiencies of the Akamatsu patent.

For the foregoing reasons, the Examiner's rejection of the pending claims under 35 U.S.C. 103(a) cannot be maintained because the motivation to combine the references is lacking, and even if the teachings of the references were combined, they fail to teach or suggest the combination of limitations recited by the respective claims. Therefore, the rejection of claims 41-67 under 35 U.S.C. 103(a) as being unpatentable over various combinations of the Akamatsu patent in view of the Hancu article, the Park article, the Meaden patent, the Matsuda patent, and/or the IBM technical disclosure must be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

Kimton N. Eng

Registration No. 43,605

Telephone No. (206) 903-8718

KNE:ajs Enclosures:

Postcard

Fee Transmittal Sheet (+ copy)

DORSEY & WHITNEY LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101-4010

(206) 903-8800 (telephone)

(206) 903-8820 (fax)

h:\ip\documents\clients\micron technology\00\500080.02\500080.02 amendment 4.doc